Marked- Up Copy of Claims

11. A structure of an Electrically Erasable Programmable Read-Only Memory (EEPROM), comprising:

a silicon substrate having a source/drain region;

a tunnel oxide layer disposed over said silicone substrate;

a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material;

a sidewall forming a single floating gate aligned to one side of said select gate;

a third insulated material disposed over said tunnel oxide layer, said select gate and said floating gate; and

a control gate formed on said third insulated material.